REMARKS

We have amended the claims to more particularly point out and distinctly claim the invention and we have added a new dependent claim 25. Upon entering the amendments presented herein, claims 1-17 and 21-25 will be pending in this application.

The Examiner rejected claims under 35 U.S.C. §112, 2nd paragraph, as omitting essential structural cooperative relationships of elements. We have amended claim 1 to supply cooperative relationships among the structural elements.

The Examiner rejected claims 1-17 and 21-24 under 35 U.S.C. §101 as being directed to non-statutory subject matter. The Examiner argues that the claimed invention does not accomplish a practical application and that it is directed to a preemption of a calculation and/or manipulation of data. We disagree.

The claims are directed to a new chip or device for performing an inverse-free Berlekamp-Massey (BM) algorithm on received code words to locate and correct errors in those code words. The "chip" has been expressed as a physical entity, that is, as a "system". That data processing system is a "machine" within the context of 35 USC 101. Moreover, we have made the physical nature of the claimed invention more clear by amending the claims to refer to the multipliers as multiplier circuits and the adders as adder circuits.

The claimed invention also has practical applications. More specifically, it is used for "determining at least one of locations and magnitudes of errors in a received code word," as now explicitly recited in the claim. The code words represent either a transmitted message or a stored data. The BM algorithm is used to generate an error-locator polynomial and an error evaluator polynomial as can be appreciated from, for example, paragraph [0013] of the present application. So, the invention of claim 1 has practical application within the fields of telecommunications or data storage.

The claims do not preempt the recited manipulations. As pointed out in the Background of the present application, "there exists various architectures for solving the key equations." The

present claims are directed to a particular hardware implementation for carrying out those manipulations, namely, one which has no more than t+1 finite multiplier circuits.

The Examiner rejected claims 1-3, 5-17, and 21-23 under 35 U.S.C. §102(e) as anticipated by U.S. 7,051,267 to Yu et al. (a.k.a. Yu).

We note that the examiner in formulating his argument has looked at only part of the circuit that Yu discloses for computing the inversionless Berlykamp-Massey algorithm (see Fig. 9). However, when taking the technical teaching of Fig. 9 in the context of the whole of the circuit it can be seen that t=3, that there are t+1 adders, and that there are 4t+1=13 multipliers. Therefore, Yu does not teach or suggest the following limitations recited in claim 1:

> A data processing system for determining at least one of locations and magnitudes of errors in received code word via respective coefficients of at least part of one of an error-locator polynomial and an error-evaluator polynomial of degree t in at least part of an inversion-free Berlekamp-Massey algorithm, wherein t is an integer...

and

> ... the data processing system includes no more than (t+1) finite field multiplier circuits.

As noted in the present application "[having] fewer multipliers has clear benefits in terms of circuit complexity, chip area, power consumption and/or circuit speed". Also, there does not appear to be any prior art which would lead one skilled in the art to depart from the technical teaching of Yu. Moreover, arbitrarily reducing the number of Yu's multipliers to (t+1) will render Yu inoperative.

At least for the reasons stated above, we believe that the claims are in condition for allowance and therefore ask the Examiner to allow them to issue.

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Respectfully submitted,

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